Form PTO 1449 (Modified) — U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

LIST OF REFERENCES CITED BY APPLICANT

ATTY DOCKET NO.	SERIAL NO.
193414US2	09/612,298
APPLICANT: Tatsuya KUNIKIYO	
FILING DATE: July 7, 2000	GROUP: 2811

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						
	AL						
	AM						
	AN						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION YES	TRANSLATION NO
PC	AO	4-179126	06/25/92	JAPAN (with partial English Translation)	X	
PC	AP	8-222632	08/30/96	JAPAN (with partial English Translation)	X	
PU	AQ	10-199882	07/31/98	JAPAN (with partial English Translation)	X	
	AR					
	AS					
	AT					
	AU					
	AV					

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, etc.)

PC	AW	T. UDEA, et al., 1999 Symposium on VLSI Technology Digest of Technical Papers, pps. 111-112, "INTEGRATION OF 3 LEVEL AIR GAP INTERCONNECT FOR SUB-QUARTER MICRON CMOS," 1999
PU	AX	S. TAKAHASHI, et al., IEDM 98, pps. 833-836, "INTERCONNECT DESIGN STRATEGY; STRUCTURES, REPEATERS AND MATERIALS TOWARD 0.1μm ULSIs WITH A GIGA-HERTZ CLOCK OPERATIONS," 1998
	AY	
	AZ	

Examiner: PHAT X. CAO — Date Considered: 12/28/01

*Examiner: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.